



# 2017 TSMC International Recruitment



- **Job openings**
  - ✓ 7nm-5nm TD Engineer, 3nm pathfinding Engineer
  - ✓ 10nm Manufacturing Process/Integration Engineer
  - ✓ QR Engineer..., and many other technical and supporting positions
- **Qualifications:** Engineering & Business background who can onboard in 2017 or early 2018.
- **Location:** Taiwan

## Interview Arrangement

*Talk with us to see how tsmc can shape your career in an unlimited way*

- Register your profile on tsmc cloud (click [here](#)), preferably uploading your resume as supplement, or email your resume directly to [claire\\_hsu@tsmc.com](mailto:claire_hsu@tsmc.com) before **April, 7<sup>th</sup>**
- Video/Phone interview will be arranged for shortlisted applicants
- More detailed job openings at [www.tsmc.com](http://www.tsmc.com) or scan the QR code



*Join us!*



# Hot Job Openings

| #  | Func | Job Title  | Job Description (Responsibility)   | Location            |
|----|------|--|--|---------------------|
| 1  | R&D  | RD Module Manager<br>(Epi/CMP/Etch/<br>Wet Clean/Thin<br>Film/Diffusion/OPC/EUV/Litho) | <ol style="list-style-type: none"> <li>1. Exploratory new materials pathfinding and research</li> <li>2. Conducting exploratory module projects independently</li> <li>3. Investigating and developing the required new module capabilities</li> <li>4. Collaboration with device team to develop modern transistor architecture</li> </ol>  | Taiwan<br>(Hsinchu) |
| 2  |      | Advanced Transistor Research Manager   | <ol style="list-style-type: none"> <li>1. Responsible for projects of advanced device technology development, device target setting, scheme definition, simulation, and characterization.</li> <li>2. Coordination among Device, Integration, and Module in R&amp;D.</li> <li>3. Planning and setting priority for execution on customer request and delivery schedule.</li> </ol> |                     |
| 3  |      | Interconnect Etch Development<br>Expert/Manager  | <ol style="list-style-type: none"> <li>1. N5 and beyond BEOL baseline etch process development, CIP, and debugging.</li> <li>2. BEOL process tools selection and qualification.</li> </ol>   |                     |
| 4  |      | Interconnect Thin-Film Development<br>Expert/Manager                                   | <ol style="list-style-type: none"> <li>1. N5 and beyond BEOL baseline thin-film process development, CIP, and debugging.</li> <li>2. BEOL process tools selection and qualification.</li> </ol>  |                     |
| 5  |      | Interconnect Integration Manager/<br>Engineer  | <ol style="list-style-type: none"> <li>1. N5 and beyond BEOL baseline process integration, test pattern design and WAT data analysis.</li> <li>2. SRAM yield improvement on BEOL issue.</li> <li>3. BEOL process reliability Qual.</li> </ol>  |                     |
| 6  |      | MRAM MTJ Manager   | <ol style="list-style-type: none"> <li>1. Technical manager in magnetic film stack design.</li> <li>2. MTJ device characterization and modeling.</li> <li>3. Advanced process &amp; MTJ device integration, window characterization.</li> </ol>  |                     |
| 7  |      | FEOL Integration Manager   | <ol style="list-style-type: none"> <li>1. Lead FEOL Integration Process Development- including OD, Poly , S/D-EPI loops</li> <li>2. Define FEOL design rules</li> <li>3. Lead FEOL test key designs in M0 and TV0</li> </ol>   |                     |
| 8  |      | Advanced CMOS Device Development<br>Manager  | <ol style="list-style-type: none"> <li>1. Lead advanced device development for future high volume manufacturing foundry technology</li> <li>2. Define device architecture and specifications meeting design rule requirements.</li> <li>3. Manage device targeting and circuit level performance KPI</li> </ol>  |                     |
| 9  |      | Advanced surface science Engineer  | <ol style="list-style-type: none"> <li>1. Analyze thin-films (semiconductors, oxides, metals), surface states, and interfacial properties in heterostructures</li> <li>2. Design and develop novel surface treatment and/or passivation methods to modify surface reactivity and morphology</li> </ol>   |                     |
| 10 |      | Nano-device Engineer   | <ol style="list-style-type: none"> <li>1. Analyze mechanical integrity of novel 3D device nano-structures for exploratory device research</li> <li>2. Collaborate with device team to design nano-devices with robust structural and mechanical integrity</li> <li>3. Develop novel strain engineering knobs for device performance enhancement</li> </ol>                         |                     |

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|----|------|--|--|------------------|
| 11 | R&D  | Quantum transport TCAD Engineer        | <ol style="list-style-type: none"> <li>1. Develop and apply fundamental quantum physics simulations to calculate band structure and carrier transport in nano-scaled and low-dimensional devices</li> <li>2. Using quantum transport models and simulations (ex: NEGF) to guide continuum TCAD model development</li> </ol>  | Taiwan (Hsinchu) |
| 12 |      | Mechanical stress TCAD Engineer        | <ol style="list-style-type: none"> <li>1. Develop and apply fundamental mechanical stress simulations to predict and model the mechanical stress of nano-scaled devices and materials</li> <li>2. Solid understanding of mechanical mechanisms of VLSI technology related materials, including stress, crystal fracture/dislocation, flowable/viscosity, and BEOL/interconnect</li> <li>3. Design innovative structures or process flow to enhance device stress for performance and stress metrology development</li> </ol>                               |                  |
| 13 |      | Advanced plasma physics Engineer       | <ol style="list-style-type: none"> <li>1. Process chamber design &amp; modification</li> <li>2. Plasma damage study</li> <li>3. Plasma/surface interaction study</li> </ol>  |                  |
| 14 |      | ALD Precursor chemistry Engineer       | <ol style="list-style-type: none"> <li>1. New precursor synthesis &amp; screening</li> <li>2. selective deposition precursor development</li> </ol>  |                  |
| 15 |      | Self-Alignment-Molecule (SAM) Engineer | <ol style="list-style-type: none"> <li>1. SAM on dielectrics or on metal</li> <li>2. SAM functional group design and screening</li> </ol>  |                  |
| 16 |      | Emerging memory Integration engineer   | <ol style="list-style-type: none"> <li>1. Emerging memory technology development, responsible for process integration, wafer handling, layout design, tape-out.</li> <li>2. WAT, yield, and reliability data analysis and improvement</li> </ol>   |                  |
| 17 |      | Emerging memory Device engineer        | <ol style="list-style-type: none"> <li>1. WAT, yield, and reliability data analysis and improvement</li> <li>2. Basic circuit analysis and familiar with DC/AC measurement and setting</li> <li>3. Bench measurement to collect single cell and related data, and array testing to collect statistical distribution data.</li> <li>4. Analyze measurement data and find out the theory behind, capable to design experiment to verify/prove the theory</li> <li>5. Propose models to explain failures and improvement plans to fix the failures</li> </ol> |                  |
| 18 |      | Advanced Device Engineer               | <ol style="list-style-type: none"> <li>1. Technology development, device simulation, test key &amp; test circuit design</li> <li>2. Characterization and documentation</li> <li>3. Task management and cross-team collaboration among device team, product and PIE, Module, SPICE, DRC/LVS/PDK</li> </ol>  |                  |

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| 19 | R&D  | Advanced Integration Engineer                       | <ol style="list-style-type: none"> <li>1. Advanced process &amp; device integration, window characterization</li> <li>2. Co-work with device and process module people to develop advanced technology</li> <li>3. WAT trouble shooting &amp; yield improvement by process optimization and technology transfer</li> <li>4. Customer technical interface, NTO and customers handling</li> </ol> | Taiwan (Hsinchu/Tainan) |
| 20 |      | Yield Engineer                                      | <ol style="list-style-type: none"> <li>1. Advanced technology development</li> <li>2. In-line inspection and defect detection, root cause analysis. Work with integration and modules to drive defect reduction</li> <li>3. In-line inspection recipe and methodology development</li> </ol>   | Taiwan (Hsinchu)        |
| 21 |      | Advanced Module Engineer (Etch/CMP/Epi/Thin-Film)   | <ol style="list-style-type: none"> <li>1. Advanced module process development and baseline sustaining</li> <li>2. Process stability/manufacturability improvement for yield and reliability qualification</li> <li>3. Process/tool transfer to volume manufacturing</li> </ol>   | Taiwan (Hsinchu/Tainan) |
| 22 |      | Extreme Ultraviolet Lithography (EUV) Mask Engineer | <ol style="list-style-type: none"> <li>1. Technology development of Mask inspection</li> <li>2. Verify the Extreme ultraviolet lithography (EUV) mask inspection criteria</li> <li>3. Reach and development E-beam inspection tool for mask defect detection</li> <li>4. Optical inspection tool verification</li> </ol>   | Taiwan (Hsinchu)        |
| 23 |      | Advanced Lithography Engineer                       | <ol style="list-style-type: none"> <li>1. Advanced lithography module process development and baseline sustaining</li> <li>2. Process stability/manufacturability improvement for yield and reliability qualification</li> <li>3. Process/tool transfer to volume manufacturing</li> </ol>   |                         |
| 24 |      | Optical Proximity Correction (OPC) Engineer         | <ol style="list-style-type: none"> <li>1. Recipe development for Optical proximity correction (OPC) recipes and multiple patterning decomposition recipes</li> <li>2. Optical proximity correction (OPC) taped-out layer sponsors</li> <li>3. Resolution enhancement technology development</li> </ol>   |                         |
| 25 |      | OPC (Optimal Pattern Correction) Senior Engineer    | <ol style="list-style-type: none"> <li>1. Software design, develop, maintain and support</li> <li>2. Application flow design and integration</li> <li>3. Progress monitor and control</li> </ol>   |                         |
| 26 |      | Backend Integration Engineer                        | <ol style="list-style-type: none"> <li>1. Process development of Si interposer, TSV, RDL, and assembly processes.</li> <li>2. Design rule verification and yield improvement</li> <li>3. Test vehicle design, mask tape out, wafer process integraton, and package assembly</li> <li>4. Reliability certification</li> </ol>   | Taiwan (Hsinchu)        |
| 27 |      | Packaging Process Engineer                          | <ol style="list-style-type: none"> <li>1. Advanced packaging module development for fan-out technology</li> <li>2. Exploratory packaging process development for new applications</li> </ol>   |                         |
| 28 |      | 3DIC Engineer                                       | <ol style="list-style-type: none"> <li>1. In charge of FPS and SoIC integration program developing</li> <li>2. Responsible for 3D IC process development.</li> </ol>   |                         |

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|----|-------------------|---|--|------------------------------------|
| 29 | R&D               | RF Device Engineer  | <ol style="list-style-type: none"> <li>1. Responsible for layout design, tape-out and wafer handling</li> <li>2. Develop RF device process and characterization</li> </ol>   | Taiwan (Hsinchu)                   |
| 30 |                   | Embedded Flash Integration Engineer                                       | <ol style="list-style-type: none"> <li>1. Embedded memory process integration</li> <li>2. Logic, HV and SRAM process and device engineering</li> <li>3. WAT analysis and yield improvement</li> <li>4. Flash reliability improvement</li> </ol>  |                                    |
| 31 | IC Design         | APR Engineer  | <ol style="list-style-type: none"> <li>1. Physical implementation of advanced technology chips</li> <li>2. Design methodology development and innovation for advanced technology challenges</li> <li>3. Be responsible for 16/10/7nm chip implementation for internal or customer projects. EDA tool enablement and customer's support if necessary.</li> </ol>  |                                    |
| 32 |                   | Process Design Kits(PDK) Engineer   | <ol style="list-style-type: none"> <li>1. Need programming ability on UNIX environment, EDA tool design flow knowledge (will have internal and external training).</li> <li>2. Help to develop the PDK on MainStream process nodes including the speciality applications.</li> <li>3. Co-work with tsmc internal teams, external customers and EDA vendors.</li> </ol>   |                                    |
| 33 | Manufa<br>cturing | Process Engineering Manager (Etch/Litho/PVD/CVD/CMP/ Diffusion/Wet Clean) | <ol style="list-style-type: none"> <li>1. Enlarge process window and defect reduction</li> <li>2. Know hardware well and deliver CIPs for defect reduction</li> <li>3. Define roadmaps and drives improvements on device, quality, reliability, cost, yield, process stability, capability, and productivity for a new technology process</li> <li>4. Improve process and equipment - quality, cycle-time, capacity &amp; cost</li> <li>5. Set up line defense system and meet tool and process matching requirements throughout start-up and ramp of new technology transfer</li> </ol> | Taiwan (Hsinchu/ Taichung/ Tainan) |
| 34 |                   | Process Integration Manager (Logic, CIS, MEMS, IR Sensor)                 | <ol style="list-style-type: none"> <li>1. Lead the team for the process integration and new product develop and ramp up</li> <li>2. New technology or customized technology transfer, installation, qualification, volume production ramping and sustaining smooth production</li> <li>3. Responsible for WAT trouble shooting, yield improvement &amp; cost reduction driving</li> </ol>  |                                    |
| 35 |                   | Process Engineer  | <ol style="list-style-type: none"> <li>1. Work with a team which may include device, integration, yield, lithography, etch and thin films or external suppliers to drive leading-edge integrated module development, control and improvements</li> <li>2. Be responsible for sustaining ownership such as day-to-day operations, equipment troubleshooting and mentoring technicians</li> </ol>  |                                    |
| 36 |                   | Process Integration Engineer  | <ol style="list-style-type: none"> <li>1. Maintain and control Inline defect baseline and excursion</li> <li>2. Responsibility for Technology yield/defect problem</li> <li>3. New technology defect study and early detection</li> </ol>  |                                    |
| 37 |                   | Equipment Engineer  | <ol style="list-style-type: none"> <li>1. Handle Diffusion, Thin Film, Lithography or Etching equipments</li> <li>2. Warm up , trouble solve, Improve and enhance the efficiency of equipments</li> <li>3. Plan and execute the analysis or defect detection projects</li> </ol>   |                                    |
| 38 |                   | Product Engineer  | <ol style="list-style-type: none"> <li>1. Involve and work with RD/Process integration/Process engineering team for yield improvement by Failure Analysis expertise</li> <li>2. FinFET device design and yield ramp-up</li> <li>3. Involve and work with RD in early stage to develop N16/N10 FinFET device</li> </ol>   |                                    |

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|----|---------------------------|--|--|----------------------------|
| 39 | Quality & Reliability     | System Reliability Manager/Director  | <ol style="list-style-type: none"> <li>1. Lead reliability department that responsible for the system level reliability development and validation from product development to the high volume manufacturing</li> <li>2. Collaborate with both internal and customer design teams to drive the hardware and software design development, test, and resolutions</li> <li>3. Work with R&amp;D to solve module, device, and product reliability issues for advanced technology development and high volume manufacturing</li> </ol>  | Taiwan (Hsinchu/ Taichung) |
| 40 |                           | Statistics Manager   | Semiconductor Process and Reliability Statistics on: <ol style="list-style-type: none"> <li>1. Develop innovative statistical process control system</li> <li>2. Validate process margin for reliability key stages.</li> <li>3. Identify and analyze key process/equipment factors to differentiate good &amp; bad materials.</li> <li>4. Develop effective sampling plan for reliability screening.</li> </ol>   |                            |
| 41 |                           | Failunce Analysis Engineer   | <ol style="list-style-type: none"> <li>1. Conduct FA service for tsmc reliability qualification failures.</li> <li>2. Conduct Physical profile check for inline or off-line analysis.</li> <li>3. Conduct the survey of "More than Moore" FA tools and develop new FA methodologies.</li> <li>4. Cooperate with RD/ PE/ Fab/ CQR and customers to resolve developing/Fab issue.</li> </ol>   |                            |
| 42 | Machine Learning Engineer | <ol style="list-style-type: none"> <li>1. Apply data science and machine learning techniques on large data sets of structured, semi-structured unstructured data to discover data insights.</li> <li>2. Collaborate with business teams (e.g. Operations, R&amp;D, and Supporting) with a healthy sense of exploration and driving business insights.</li> <li>3. Evaluate and develop new data analysis solutions based on predictive, behavioral or other models via statistical analysts and use of relevant modeling techniques</li> </ol> |  |                            |
| 43 | IT                        | Big Data Analyst   | <ol style="list-style-type: none"> <li>1. Work on large data sets of structured, semi-structured unstructured data to discover data insights and collaborate with business partners to deliver business value through these insights.</li> <li>2. Combine strengths in data management, analysis, applied statistics, visualization capabilities</li> <li>3. Ability to work with business teams (e.g. Operations, R&amp;D, Supporting) with a healthy sense of exploration and driving business insights.</li> <li>4. Develop data analysis solutions based on predictive, behavioral or other models via statistical analysts and use of relevant modelling techniques.</li> <li>5. Collaborate with engineering, architecture, Big Data solution team, and other teams to ensure that requirements for integration, security, data quality and cross functional usage are addressed.</li> </ol> |                            |
| 44 |                           | Information Security Engineer  | <ol style="list-style-type: none"> <li>1. Develop or lead in technical solutions to mitigate security vulnerabilities.</li> <li>2. Perform security design review for IT applications.</li> <li>3. Enhance Security Operations Center efficiency and effectiveness.</li> </ol>   |                            |

| #  | Func     | Job Title                       | Job Description (Responsibility)   | Location                                    |
|----|----------|---------------------------------|--|---|
| 45 | HR       | HR Specialist                   | <p>1. Employee champion to create the working environment with balanced of work life and belonging</p> <ul style="list-style-type: none"> <li>- Implement the function/fab's annual learning and development plans to meet the professional, operational and organizational needs</li> <li>- Facilitate the need identification and analysis for special or customized development plan to close performance discrepancies</li> </ul> <p>2. Change agent as identify issue, diagnostic situation , initiate idea and action plan to help the organization execute the necessary change</p> <ul style="list-style-type: none"> <li>- Identify gaps associated with organizational changes – people, processes, best practices – and facilitate the development and implementation of people and organization development programs</li> <li>- Promote and facilitate the development, especially among new teams and employees</li> </ul> <p>3. Services provider on the daily basis to serve the employees and business partners.</p> <ul style="list-style-type: none"> <li>- Take ownership, evaluate and ensure the relevance and effectiveness of various employee services programs in alignment with business principle of a fun and dynamic working environment</li> <li>- Establish team/organization capability bench strength charts and profiles for organization development</li> </ul> | Taiwan<br>(Hsinchu/<br>Taichung/<br>Tainan) |
| 46 | Finance  | Corporate Finance Associate     | <p>1. Rotate among 2~3 functions within a timeframe of 3 years+. Such functions include treasury operations, Financial Planning, Customer Credit, Insurance, Financial Risk Management, SEC Compliance and Investment Management</p> <p>2. Job scope includes funding, FX risk management, debt/equity offerings, investment valuation, various projects to support management decisions, credit risk management, multiple insurance programs to reduce TSMC's operating risk, financial risk control/modeling, ROC/US SEC compliance, and post-investment management</p>  | Taiwan<br>(Hsinchu)                         |
| 47 |          | Credit Analyst, Customer Credit | Account management, customer credit analysis, accounts receivable management, and projects deemed necessary to support management decisions.   |   |
| 48 | Legal    | Patent Litigation Attorney      | Day-to-day oversight of outside counsel, active management of all litigation activities, developing internal discovery strategy and overall case strategy, attending depositions and hearings, and conducting internal education and training.   |   |
| 49 |          | Patent Attorney                 | <p>1. Work with technical and legal teams to formulate favorable positions in IP disputes.</p> <p>2. Coordinate legal actions related to IP disputes including IPR, discovery deposition, etc.</p> <p>3. Do IP assessment and technology analysis for patent acquisition.</p> <p>4. Coach inventors to generate valuable intangible assets.</p> <p>5. Review draft patent applications and related patent prosecution documents.</p>   |   |
| 50 | Business | Procurement Engineer            | Semiconductor manufacturing materials sourcing, purchasing, supply chain risk management and cost reduction.   |   |

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|----|-----------|--|---|------------------|
| 51 | Business  | Fab Production Control Planner   | <ol style="list-style-type: none"> <li>1. Fab production planning: Capacity support and customer demand fulfillment; bolster technology developing/ramping/production &amp; business engagement</li> <li>2. Fab operation management: NTO pilots and priority lots management, production delivery management, CT management and key bottleneck tool performance monitor</li> <li>3. Operation KPI monitor and achievement</li> </ol> | Taiwan (Hsinchu) |
| 52 |           | Fab Rationalization Engineer   | <ol style="list-style-type: none"> <li>1. Demand to supply rationalization, maximize capacity utilization</li> <li>2. Analyze product and new tape out portfolio for fab utilization effectiveness</li> <li>3. Provide FR proposal to optimize fab loading and customer's requirement</li> </ol>  |                  |
| 53 | IC design | VLSI Design Analysis Engineer  | Analyze various industrial VLSI design views from RTL to GDSII and extract key design metrics with efficient algorithms, and turn them into useful guidance for future designs optimization and process technology offerings.   | China (Nanjing)  |
| 54 |           | Front-End Design Engineer  | <ol style="list-style-type: none"> <li>1. Advance process test chip design.</li> <li>2. Take the responsibility and have the capability to implement the test chip individually which includes design for test, logic synthesis and verification.</li> </ol>  |                  |
| 55 | FAC       | Facility Engineer (Mechanical /Electrical/ Instrument/ Water/GAS/Chemical) | <ol style="list-style-type: none"> <li>1. Should capable of conducting work shifts.</li> <li>2. Maintenance and improvement of the facility mechanical /electrical and instrument/Water/GAS/Chemical system.</li> <li>3. Engineering management &amp; Project coordination.</li> <li>4. Provide a stable/Specific facility system to fulfill wafer production requirement.</li> </ol>   |                  |