TAIWAN AND THE GLOBAL SEMICONDUCTOR SUPPLY CHAIN

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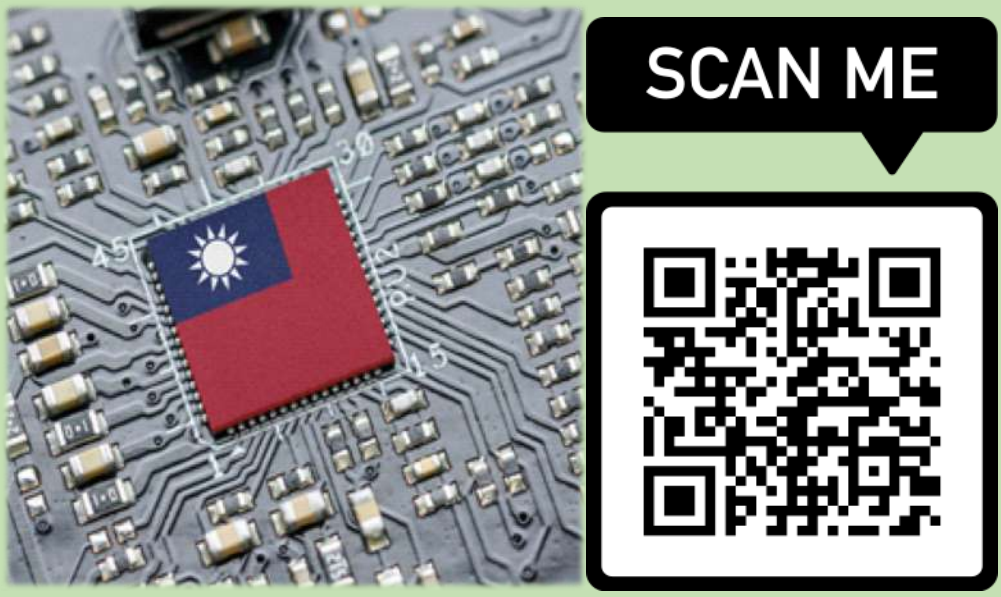
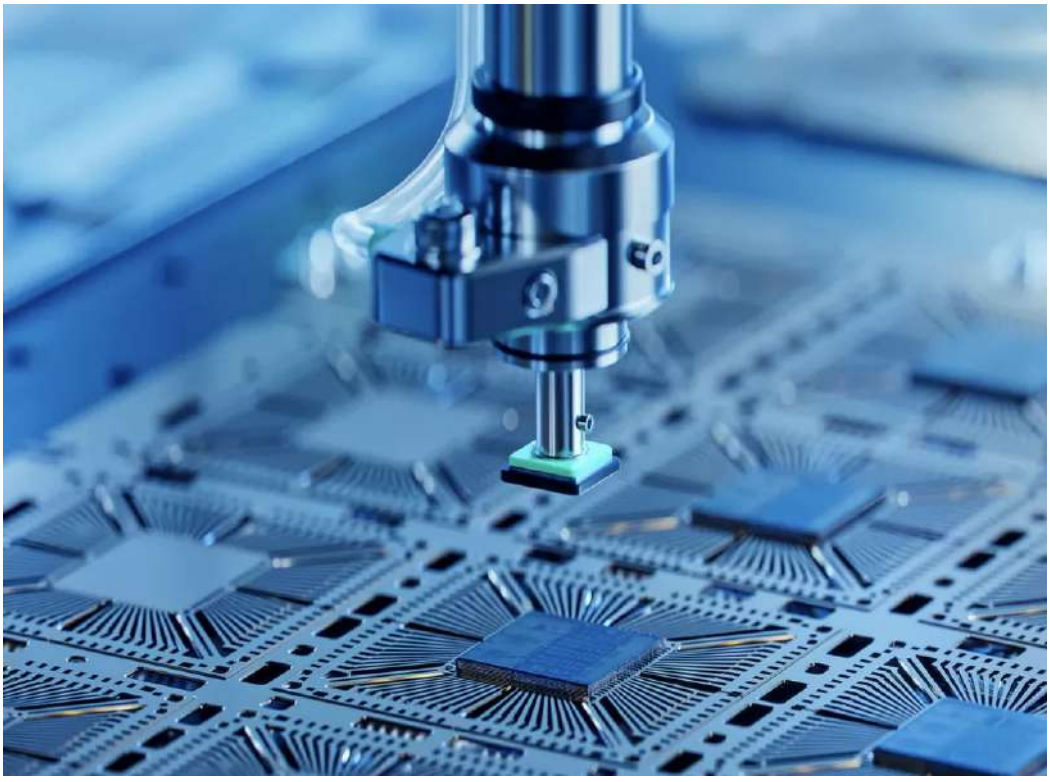


IN THE SPOTLIGHT

Advanced Semiconductor Packaging and Testing

- **As the benefits of Moore's law reach their limits, advanced semiconductor packaging has emerged as a significant pathway for producing more powerful chips.**
- **TSMC, Intel, and Samsung have emerged as the key innovators of new advanced semiconductor packaging technologies.**
- **More players are jumping on the advanced semiconductor packaging bandwagon as advanced packaging offers a higher-value opportunity than traditional back-end packaging.**
- **Advanced semiconductor packaging technologies are expected to account for 58% of the semiconductor packaging market by 2028, up from 47% in 2022.**



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OVERVIEW

Semiconductors are an essential component of electronic devices and power our modern digital world. Increasingly, countries see it as an imperative to invest heavily in semiconductor innovation to produce more powerful and cost-effective chips as a means to advance their growth, competitiveness, and

national security.[1] However, as the benefits of Moore's Law, which predicts the doubling of transistors in a dense integrated circuit approximately every two years, are reaching their limits, advanced semiconductor packaging has become a valuable tool for enhancing product value.[2] At a time when traditional strategies for innovation are becoming increasingly complex and costly to manufacture, industry leaders such as Taiwan Semiconductor Manufacturing Company (TSMC), Intel Corp, and Samsung Electronics see leadership in advanced packaging as an important pillar for semiconductor innovation.[3]

What is Semiconductor Packaging?

The semiconductor production process involves three general steps: design, fabrication, and assembly, testing, and packaging (ATP). After individual components have been designed and are fabricated on silicon wafers, ATP involves the use of specialized equipment and materials to dice the wafers into individual chips (assembly), test the chips for operability (testing), and finally encase the fabricated chips in various materials such as metal, glass, or plastic (packaging). [4]

Packaging serves two general purposes. The first is to protect the chip mechanically, thermally, and environmentally. The second is to facilitate reliable inter-chip communication, deliver power, and provide a stable test and system integration platform.[5] Packaging is, therefore, an important part of ensuring that chips function as intended when they leave the manufacturing facility for use in different electronic applications.[6] Additionally, while ATP are

[1] Sujai Shivakumarand Chris Borges, "Advanced Packaging and the Future of Moore's Law," Center for Strategic and International Studies, June 26, 2023.
[2] Ibid; Mordor Intelligence, "Semiconductor Packaging Market Size & Share Analysis - Growth Trends & Forecasts (2023 - 2028)," December 22, 2023.
[3] TSMC, Advanced Packaging Services, 2024, https://www.tsmc.com/english/dedicatedFoundry/services/advanced-packaging; Samsung, Advanced Package, 2023, https://semiconductor.samsung.com/foundry/advanced-package/; Intel, Semiconductor Chip Packaging, 2023, https://www.intel.com/content/www/us/en/foundry/packaging.html.
[4] John VerWey, Policy Brief: "Re-Shoring Advanced Semiconductor Packaging Innovation, Supply Chain Security, and U.S. Leadership in the Semiconductor Industry," Centre for Security and Emerging Technology, June 2022; Sujai Shivakumarand Chris Borges, "Advanced Packaging and the Future of Moore's Law," Center for Strategic and International Studies, June 26, 2023.
[5] CHIPS Research and Development Office, National Institute of Standards and Technology, "The Vision for the National Advanced Packaging Manufacturing Program," November 20, 2023.
[6] Industry Growth Insights, "Global IC Packaging and Packaging Testing Market - Industry Analysis, Growth, Share, Size, Trends, Key Regions and Forecast From 2022 to 2030," June 26, 2023.

distinct steps in the semiconductor fabrication process, they are often performed sequentially by the same firms at the same facilities in the same region(s) of the world, and are therefore grouped together.[7]

With Moore's Law becoming more challenging; demands of electronic products with smaller size, more powerful performance and lower cost growing; the need for improved connectivity rising; and a surge in the use of high-performance chips requiring better heat dissipation, there is a growing shift towards prioritizing advanced packaging. In addition, advanced packaging offers a higher-value opportunity than traditional back-end packaging, and more players are jumping on the advanced semiconductor packaging bandwagon.

What is Advanced Packaging?

Advanced packaging is a subset of traditional packaging. It is not one specific packaging technique, but rather an array of technologies and capabilities that allow the combination of multiple chips and other components to form a highly integrated, multi-functional sub-system which can then be assembled onto laminates, panels, or circuit boards. Advanced packaging is categorized as front-end 3D which stacks chips or wafers vertically and back-end 2.5D Chip-on-Wafer-on-Substrate (CoWoS) that interconnects dies horizontally via a redistribution layer (RDL) or interposer.[8] Compared to conventionally packaged chips on a printed circuit board, advanced packaging achieves greater function, performance, and power savings.[9]

GLOBAL SEMICONDUCTOR PACKAGING AND TESTING INDUSTRY

Integrated circuit (IC) assembly, testing, and packaging (ATP) services occur under two business models: (1) by outsourced semiconductor assembly and test (OSAT) firms, which perform ATP for third-party customers; and (2) as in-house ATP services performed by integrated device manufacturers (IDMs)

[7] John VerWey, Policy Brief: "Re-Shoring Advanced Semiconductor Packaging Innovation, Supply Chain Security, and U.S. Leadership in the Semiconductor Industry," Center for Security and Emerging Technology, June 2022.
[8] Counterpoint, "AI Chip Market: Advanced Packaging Capabilities Key Differentiating Factor," July 24, 2023.
[9] National Institute of Standards and Technology, Department of Commerce, United States, "National Advanced Packaging Manufacturing Program", November 20, 2023.

and foundries after fabrication. Firms headquartered in Taiwan, the United States, China, and South Korea are the main providers of ATP services.[10]

Major Players in Semiconductor Packaging and Testing Industry

Foundries like TSMC, integrated device manufacturers (IDMs) such as Intel and Samsung, and outsourced semiconductor assembly and test (OSAT) companies are important players in the global semiconductor packaging and testing industry.[11]

The global semiconductor packaging and testing industry is largely dominated by OSAT companies. These firms specialize in providing third-party integrated circuit (IC) packaging and testing services, including wafer bumping, wafer probing, IC packaging, and IC testing. The global top two OSAT companies are Taiwan's Advanced Semiconductor Engineering (ASE) Technology Holding and US-headquartered Amkor Technology.[12]

Figure 1 shows the global OSAT revenue and growth trend for 2020 to 2027. The OSAT industry grew steadily in 2022 and worldwide OSAT revenue reached a high of US$ 42.6 billion, an annual growth of 7.6%. This record OSAT revenue is attributed to a surge in global demand for applications such as artificial intelligence (AI), high-performance computing (HPC), 5G, automotive, and Internet of Things (IoT) that fueled the semiconductor supply chain expansion.[13]

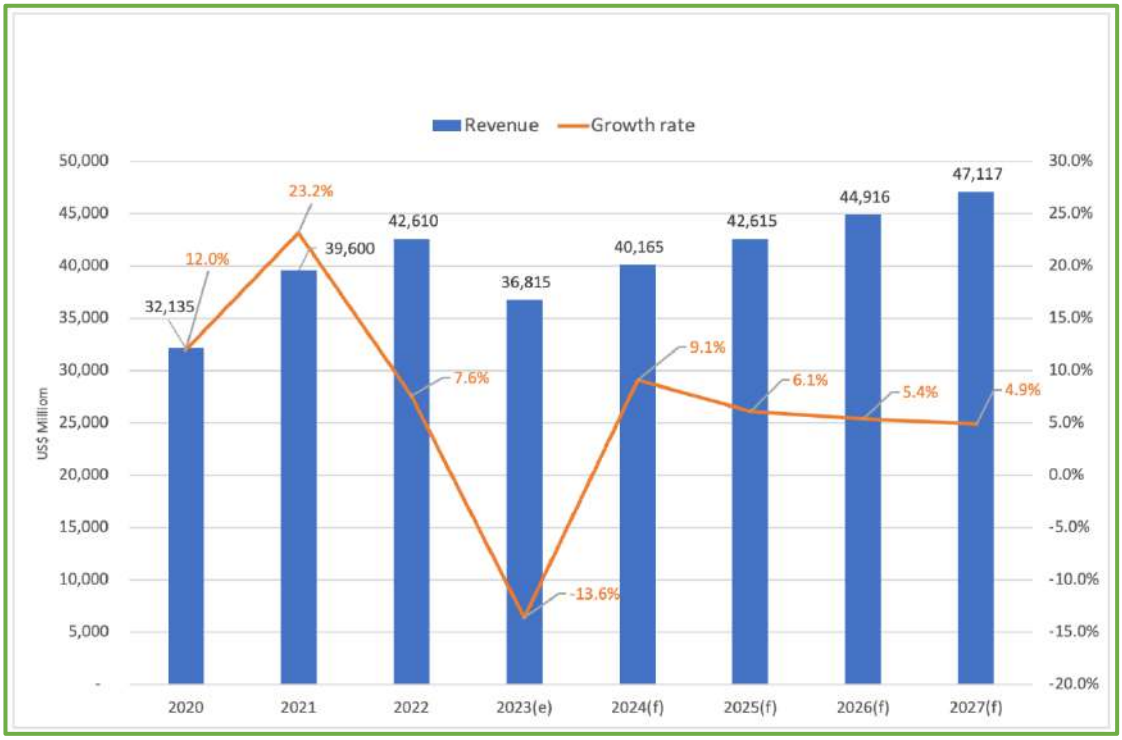
In 2023, an oversupply of chips due to inventory accumulation as well as geopolitical and global economic uncertainties contributed to weakened consumer demand, and the global OSAT revenue was forecasted to decline by 13.6% to US$ 36.8 billion.

The global semiconductor market will experience a revival in 2024 with an estimated growth of 13.1%, according to World Semiconductor Trade

[10] David Manners, "OSAT market set to fall 13.3% in 2023," Electronics Weekly, August 1, 2023.
[11] Trendforce, "Chinese Semiconductor Design Industry Diverts to Malaysia to Evade U.S. Controls; Potential Advanced Packaging Orders Surge for ASE," December 19, 2023.
[12] Ibid.
[13] IDC, Press Release: "IDC: Worldwide Semiconductor OSAT Market Grew 5.1% YoY in 2022, Growth Expected in 2024 Due to Accumulated Advanced OSAT Demand," July 25, 2023.

Statistics (WSTS).[14] As consumer demand gradually stabilizes and electronic product inventory becomes depleted, the global OSAT revenue is also expected to begin to recover and reach US$ 40.2 billion in 2024. This upward trend is expected to steadily continue through to 2027.

Figure 1: Global Outsourced Semiconductor Assembly and Test Revenue and Growth Trend: 2020-2027



Source: Yunnie Chang, "The Sustainable Management of Semiconductor Packaging and Testing," IEK, ITRI, October 30, 2023, p.8.

Semiconductor packaging and testing is largely a labor-intensive process involving precise handling, assembly, and inspection of tiny and delicate semiconductor devices. To take advantage of lower wages and input costs, a significant portion of the world's assembly, testing, and packaging (ATP) production is located in Asia. For example, U.S. semiconductor firms often offshore nearly all packaging processes to outsourced semiconductor assembly and test (OSAT) companies or rely on integrated device manufacturer (IDM) facilities owned by U.S. companies that are located overseas.[15]

[14] World Semiconductor Trade Statistics (WSTS), News Release: "WSTS Semiconductor Market Forecast Fall 2023," November 28, 2023.

[15] Hideki Tomoshige, "CHIPS+ and Semiconductor Packaging," Center for Strategic and International Studies, November 7, 2022.

Advanced packaging plays a significant role in enhancing the performance, functionality, and form factor of electronic devices. As such, advanced packaging is not only an important step, but also a driving force in semiconductor innovation. Recent advances in artificial intelligence, for example, would not be possible without advanced packaging.[16]

Based on gross profit margin and cost factors, leading wafer fabs and outsourced semiconductor assembly and test foundries still largely focus on Asian countries in setting up advanced packaging sites.[17] Taiwan, the leader in the advanced semiconductor packaging industry, is home to TSMC (Taoyuan, Hsinchu, Zhunan, Tongluo, Taichung and Tainan), ASE (Zhongli and Kaohsiung), and Amkor (Taoyuan and Hukou). China is home to Samsung (Suzhou), ASE (Jiangsu) and Amkor (Shanghai) while South Korea is home to Samsung (Onyang), ASE (Gyeonggi-do) and Amkor (Gwangju and Incheon). The ASEAN countries of Vietnam (Huyện Yên Phong) and the Philippines (Biñan) house Amkor's advanced packaging factories while Malaysia is home to advanced packaging factories owned by Intel and ASE. Outside of Asia, the U.S.A. (New Mexico) is home to Intel's advanced packaging factory (see Figure 2).

Figure 2: Distribution of Current Advanced Packaging Factories

Source: Yunnie Chang, "The Sustainable Management of Semiconductor Packaging and Testing," IEK, ITRI, October 30, 2023, p.11.
Acknowledgement: Map illustration is created by Orderble Co., Ltd.

[16] Ibid.
[17] Ibid.

By one estimate highlighted by the U.S. Department of Commerce, North America accounted for only 3% of global advanced packaging production as of 2021.[18] In its push to build up the U.S. semiconductor industry, including building a robust domestic advanced capability in the United States, approximately US$ 3 billion in funding for the National Advanced Packaging Manufacturing Program (NAPMP) will be used to drive U.S. leadership in advanced packaging.[19] The National Institute of Standards and Technology (NIST), which oversees the NAPMP program, envisions that America will both manufacture and package the world's most sophisticated chips within a decade.[20]

In addition to bolstering semiconductor production at home, the U.S.A. is also curbing Beijing's access to leading-edge chips as part of U.S. President Joe Biden's two-pronged approach to constrain China's high-tech progress.[21] In the ongoing U.S.-China contest for technological supremacy, the process of packaging semiconductors is increasingly seen as a path to achieving higher performance. Consequently, a growing number of Chinese semiconductor design companies are hedging their risks against any future expansion of U.S. sanctions on China's semiconductor industry by tapping Malaysian firms to assemble a portion of their high-end chips.[22]

TSMC - A Pioneer and Trendsetter in Advanced Semiconductor Packaging

TSMC, the world's largest semiconductor manufacturer with a market share of about 55%, is also the producer of the world's most advanced chips.[23] To stay ahead of the competition as Moore's Law slows nanometer node progress, TSMC has been seeking technological gains from innovations in both process and packaging.

[18] IPC, Summary Report: "An Analysis of The North American Semiconductor and Advanced Packaging Ecosystem- Rebuilding U.S. Capabilities for the 21st Century," November 2021.

[19] National Institute of Standards and Technology (NIST), U.S. Department of Commerce, "CHIPS for America Releases Vision for Approximately $3 Billion National Advanced Packaging Manufacturing Program," November 20, 2023.

[20] Ibid.

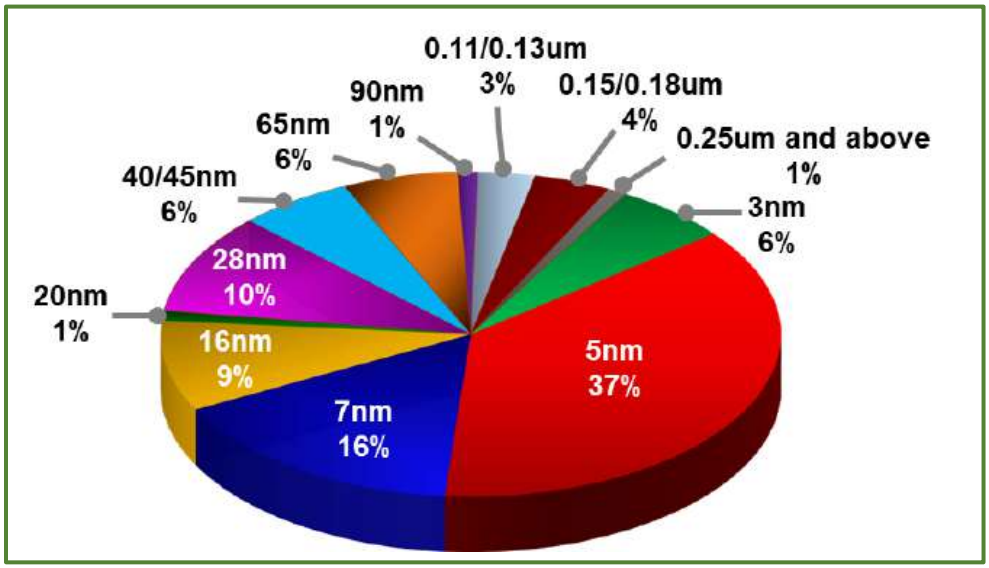
[21] Jane Lanhee Lee, Ian King, Mackenzie Hawkins, and Jillian Deutsch, "A New Front Is Opening Up in the US-China Conflict Over Chips," Bloomberg, November 21, 2023.

[22] Fanny Potkin and Yantoultra Ngui, "Exclusive: Chinese firms look to Malaysia for assembly of high-end chips, sources say," Reuters, December 19, 2023.

[23] Chang Chien-chung and Frances Huang, "TSMC cements global lead as market share rises to 57.9% in Q3," Focus Taiwan, December 9, 2023; Lisa Wang, "TSMC says new chips to be world's most advanced," Taipei Times, May 12, 2023.

Advanced chips, defined as 7 nanometers and below, have contributed to a growing share of TSMC's wafer revenue. In the third quarter of 2023, it accounted for 59% share of TSMC's wafer revenue (see Figure 3), up 7 percentage points from 52% share in the same period in 2021.[24] The most advanced technology currently being used by TSMC to make chips is the 3 nm process, which entered mass production in late 2022. It expects to begin producing chips using the 2 nm process in 2025. Beyond the 2 nm technology, TSMC is also developing a 1.4 nm process to maintain its lead over its peers in the global market.

Figure 3: Revenue Composition of TSMC: 2023Q3



Source: TSMC, 2023 Third Quarter Earnings Conference, October 2023.

Advanced semiconductor packaging is vital for squeezing maximum performance from the latest chip designs. TSMC has been investing heavily in advanced semiconductor packaging, and its cache of 2,946 advanced packaging patents is the most expansive. Its lead is followed by Samsung (2,404) and then Intel (1,434), according to data from LexisNexis.[25]

TSMC's advanced packaging services, known as 3DFabric™, offer solutions that allow customers to design their products more holistically as a system of mini-chips. This provides key advantages over designing a larger monolithic die.[26] 3DFabric™ consists of both front-end and back-end

[24] TSMC 2021 Third Quarter Earnings Conference, October 14, 2021; TSMC 2023 Third Quarter Earnings Conference, October 19, 2023.
[25] Max A. Cherney, "TSMC leads in advanced chip packaging wars, LexisNexis patent data says," Reuters, August 2, 2023.
[26] TSMC 3DFabric, https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/3DFabric.htm

technologies, including TSMC-SoIC® (System on Integrated Chip), CoWoS® (Chip-on-Wafer-on-Substrate), and InFO (Integrated Fan-Out). These technologies help resolve heterogeneous packing issues, such as chip-packaging-integration (CPI) issues, through intense collaboration with substrate, memory, and materials suppliers.[27]

TSMC's InFO and CoWoS packaging technologies are currently used for chips like Apple's M2 Ultra, AMD's Instinct MI300, and NVIDIA's A100 and H100 graphic processing units. The demand for TSMC's CoWoS is skyrocketing as the demand for advanced packaging technology in artificial intelligence (AI) and high-performance computing (HPC) domains escalates.[28] For leading tech companies such as Apple, Tesla, Google, and Meta, high-performance chips packaged using CoWoS technology provides a best possible solution as they continue to add a plethora of AI capabilities to their products and also need to provide integrated AI computing to their portfolios.[29]

TSMC's CoWoS packaging technology involves two stages: chip-on-wafer (CoW) and on-Substrate (oS). The CoW phase merges various logic ICs (central processing units, graphics processing units, and application-specific integrated circuits) and High Bandwidth Memory (HBM); the oS stage uses solder bumps to connect the CoW assembly and attach it onto a substrate. This is subsequently integrated into a server motherboard to create an AI platform with network equipment, memory subsystems, power sources, and other components.[30]

As part of its strategy to provide one-stop services to its clients, TSMC currently runs five high-end back-end semiconductor packaging and testing plants in addition to its pure wafer foundry operations in Taiwan (see Figure 4). TSMC's newly opened Advanced Backend Fab 6, for example, can process more than 1 million 12-inch wafer equivalent 3DFabric process technology per year, and more than 10 million hours of testing services per year.[31]

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[27] TSMC Advanced Packaging Services, https://www.tsmc.com/english/dedicatedFoundry/services/advanced-packaging.

[28] Trendforce, "TSMC's CoWoS Demand Surges from NVIDIA, Apple, AMD, Broadcom, Marvell, Monthly Capacity Up 120% in 2024," November 13, 2023.

[29] Science and Technology Industry Information Room, National Applied Research Laboratories, Taiwan, "With the rise of AI and HPC, CoWoS will play a key role in advanced packaging," https://iknow.stpi.narl.org.tw/post/Read.aspx?PostID=19884.

[30] TSMC Advanced Packaging Services, https://www.tsmc.com/english/dedicatedFoundry/services/advanced-packaging, 2024.

[31] TSMC, Press Release: "TSMC Announces the Opening of Advanced Backend Fab 6, Marking a Milestone in the Expansion of 3DFabric™ System Integration Technology," June 6, 2023.

Figure 4: Allocation of TSMC's Advanced Packaging and Testing Fabs

	Location	Process
Advanced Backend Fab 1	Hsinchu Science Park	Testing and back-end packaging
Advanced Backend Fab 2	Southern Taiwan Science Park	Testing and front-end 3D Fabric
Advanced Backend Fab 3	Longtan District, Taoyuan City	3D Fabric
Advanced Backend Fab 5	Central Taiwan Science Park	Testing and back-end packaging
Advanced Backend Fab 6	Zhunan Town, Miaoli County	3D Fabric, SoIC

Source: https://www.ctee.com.tw/news/20230609700288-430502?fbclid=IwAR0qgTUDfA25I4CZbN9MMTpwixHpLigozEz9vodOA9t-znyxmZsy3lhxIus_aem_Afan7qyoS3-tNlEDwvvFCNzInXyyUNysg1aQhjz2NluWJ1fRhFmeP98VvgqipQJbX7g

On July 25, 2023, TSMC announced its plans to invest about NT$ 90 billion (US$ 2.88 billion) to build an advanced semiconductor packaging and testing plant in the Tongluo Township of the Hsinchu Science Park.[32] The hefty US$ 2.88 billion price tag implies that this will be yet another significant capital expansion project for TSMC – rivaling what would have been the cost of a wafer lithography fab a decade ago. Given TSMC's product roadmaps as well as projections for the growing need for advanced packaging types in the coming years, the new semiconductor packaging plant will likely be a comprehensive facility offering 3DFabric integration of front-end to back-end processes, as well as testing services.[33]

TrendForce notes that due to robust demand, TSMC's monthly CoWoS capacity is projected to hit 12,000 wafers by the end of 2023. The demand for CoWoS has surged by almost 50% since the onset of 2023, driven by the needs of Nvidia's A100 and H100 and associated AI servers. This strong demand is anticipated to continue into 2024, with a projected growth of about 30 to 40% in advanced packaging capacity, given the readiness of related equipment.[34]

Although a market leader in advanced semiconductor packaging and testing, TSMC does not have plans to take business away from its traditional OSAT partners. Instead, it wants these companies to expand their sophisticated packaging capacity and use tools similar to TSMC's to package

[32] Chang Chien-chung and Frances Huang, "TSMC to spend NT$90 billion on advanced IC packaging, testing plant," Focus Taiwan, July 25, 2023.
[33] Anton Shilov, "TSMC to build $2.87 billion facility for advanced chip packaging," AnandTech, July 25, 2023.
[34] Frank Kung, "Major CSPs Aggressively Constructing AI Servers and Boosting Demand for AI Chips and HBM, Advanced Packaging Capacity Forecasted to Surge 30~40% by 2024, Says TrendForce," Trendforce, June 21, 2023.

TSMC-chiplets. So far, TSMC has certified two OSATs to perform the final CoWoS assembly for TSMC-made chiplets.[35]

MARKET TRENDS

Currently, the semiconductor packaging and testing market is dominated by traditional packaging platforms. Of the global market size of US$ 95 billion in 2022, the advanced packaging industry held a market size of US$ 44.3 billion, or 47% of the semiconductor packaging industry (see Figure 5).

Figure 5: Global Market Share of Advanced Packaging: 2022

Source: Yunnie Chang, "The Sustainable Management of Semiconductor Packaging and Testing," IEK, ITRI, October 30, 2023, p.14.

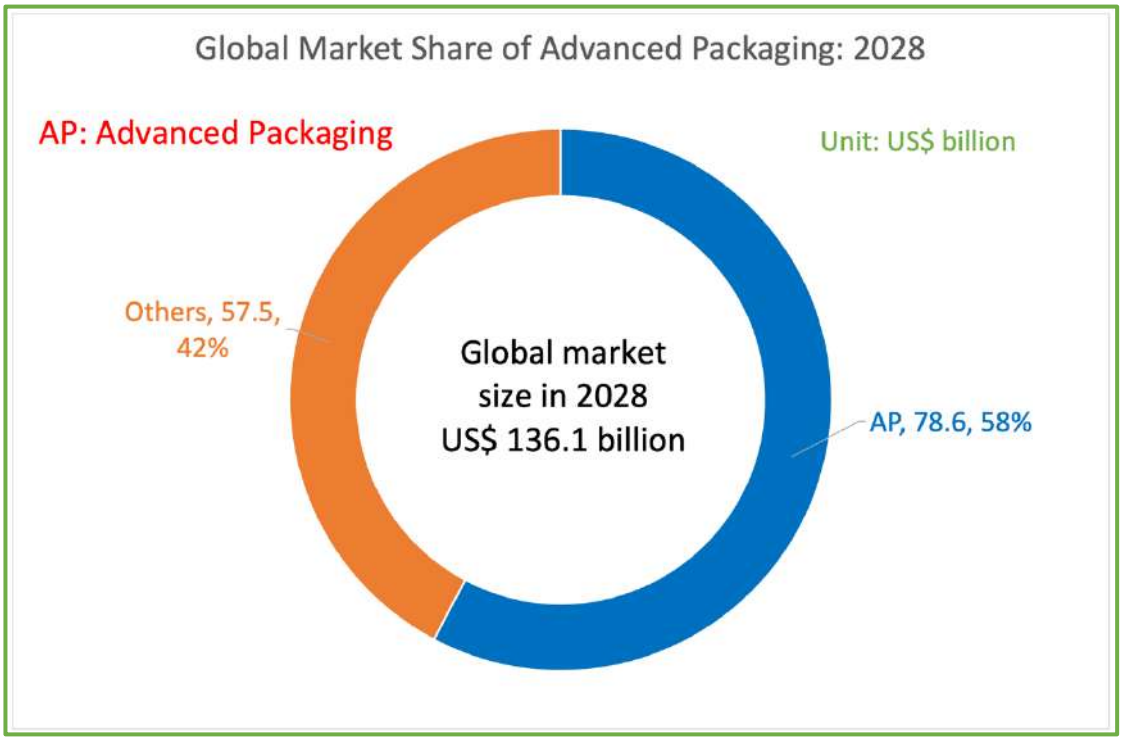
The artificial intelligence (AI) boom has driven the development of high-performance computing chips (HPC) and sparked the demand for advanced semiconductor packaging technologies. Demand for advanced packaging by AI chipmakers, like Nvidia and AMD, is skyrocketing as they seek to improve chip performance.

Consequently, the advanced packaging market is rapidly catching up with the traditional packaging market, and it is expected that the advanced

[35] Anton Shilov, "TSMC: We want OSATS to expand their advanced packaging capability," AnandTech, October 16, 2023.

packaging portion of the total semiconductor packaging market will increase from 47% in 2022 to 58% in 2028, with a compound annual growth rate (CAGR) of 10%. In fact, the whole semiconductor packaging market is expected to reach US$ 136.1 billion by 2028 (see Figure 6).

Figure 6: Global Market Share of Advanced Packaging: 2028



Source: Yunnie Chang, "The Sustainable Management of Semiconductor Packaging and Testing," IEK, ITRI, October 30, 2023, p.14.

Given the rapidly expanding demand for advanced packaging, it is unsurprising that leading chipmakers and OSAT companies are investing in new technologies and expanding their capabilities to meet the growing demand for advanced packaging solutions.

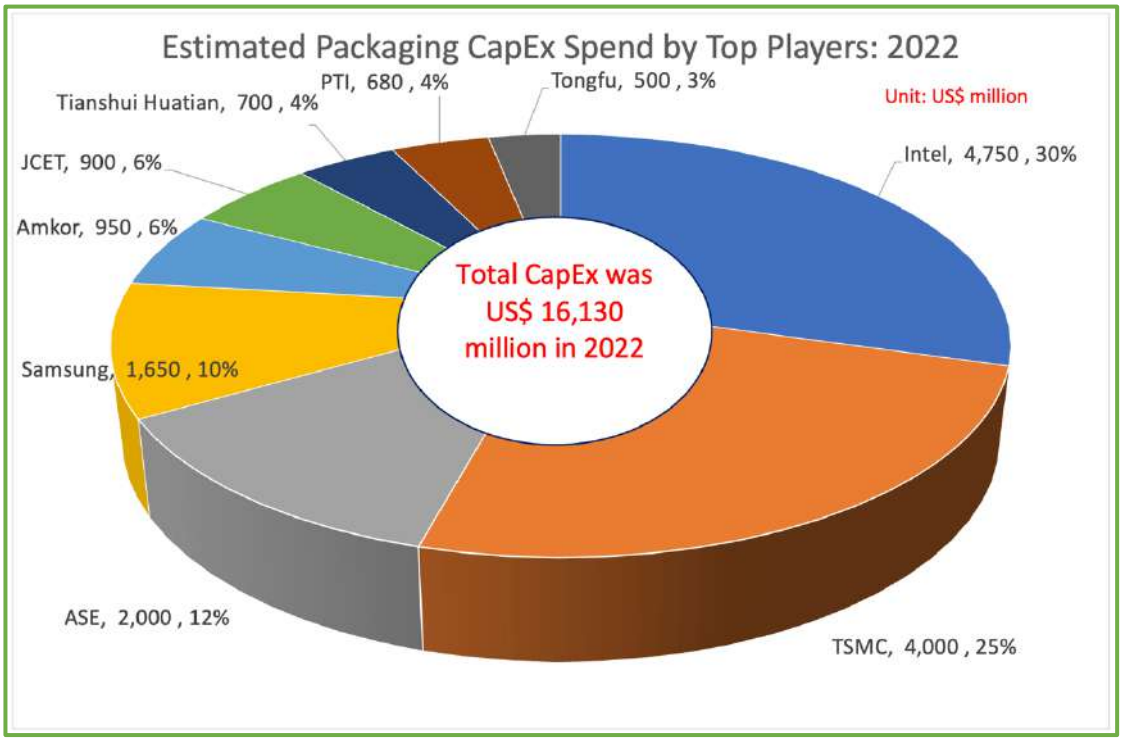
Figure 7 shows the estimated packaging capital expenditure (CapEx) by top players in 2022. The top nine players in the packaging and testing industry had an estimated packaging Capex spending of US$ 16,130 million in total in 2022.

Intel, TSMC and ASE were the leaders in capital expenditure in the semiconductor packaging and testing industry in 2022. Intel was projected to lead the market with its US$ 4.75 billion investment, followed by TSMC with about US$ 4 billion. Intel and TSMC had the highest levels of capital

expenditure, accounting for 30% and 25% of the total Capex among the top players. Meanwhile, Taiwan's ASE, the world's largest OSAT company, was the most aggressive OSAT company in its advanced packaging capital expenditure with an investment of US$ 2 billion, or 12% of the total Capex among the top players in 2022.

In view of yield risks and profit considerations, the investment of other OSAT factories was relatively conservative. U.S.-headquartered Amkor, another leading OSAT company, was expected to invest US$ 950 million. China-headquartered OSAT companies, Jiangsu Changjiang Electronics Technology Co., Ltd (JCET), Tianshui Huatian and Tongfu had CapEx spending of US$ 900 million, US$ 700 million, and US$ 500 million respectively. Meanwhile, Taiwan's Powertech Technology Incorporated (PTI)'s estimated packaging CapEx was estimated at US$ 680 million in 2022 (see Figure 7).

Figure 7: Estimated Packaging CapEx Spend by Top Players in 2022



Source: Yunnie Chang, "The Sustainable Management of Semiconductor Packaging and Testing," IEK, ITRI, October 30, 2023, p.15.

Future Prospects

The future of advanced semiconductor packaging is promising. Advanced packaging technologies are expected to account for more than 58% of the semiconductor packaging market by 2028. This shift indicates a move away from traditional packaging platforms towards more innovative solutions that can meet the demands of modern electronics.

Advanced semiconductor packaging is a dynamic and rapidly evolving field. It is a key driver in the evolution of semiconductor products, offering benefits such as increased functionality, improved performance, and cost reduction. As technology continues to advance, the importance of advanced packaging in the semiconductor industry is set to grow even further.

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TaiwanPlus Videos on Semiconductors

2023/12/11
Taiwan Talks

TSMC's Role in Global Revival: Steering Success Amid Competition, Taiwan Talks EP253

Forecasts for 2024 suggest a resurgence in the semiconductor market, driven by ongoing demand for AI and high-performance computing. This episode of Taiwan Talks highlights key trends, including advancements at TSMC and Nvidia and U.S.-China competition, as well as the development of Foxconn-STMicro chip fabs in India.

2023/12/4
Taiwan Talks

China’s Economic Challenges and Resilience, Taiwan Talks EP248

The show focuses on China's economic slowdown and its potential impact on neighboring countries, particularly in relation to the **semiconductor** industry. It discusses the implications of China's real estate sector stagnation and its effect on other developing Asian countries, as well as the shift of Western companies from China to Southeast Asia and its impact on the **global semiconductor** industry. The video also highlights Taiwan's strategies to maintain its competitive advantage in the **semiconductor** market.

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SEMICONDUCTOR STATISTICS AT A GLANCE

GLOBAL TRENDS

Figure 8: Prospects of Global Semiconductor Market: 2011-2026

Source: Chia-Chen Lee, "Global Economy and Semiconductor Market Trends in the Third Quarter of 2023," IEK, ITRI, December 15, 2023, p. 9.

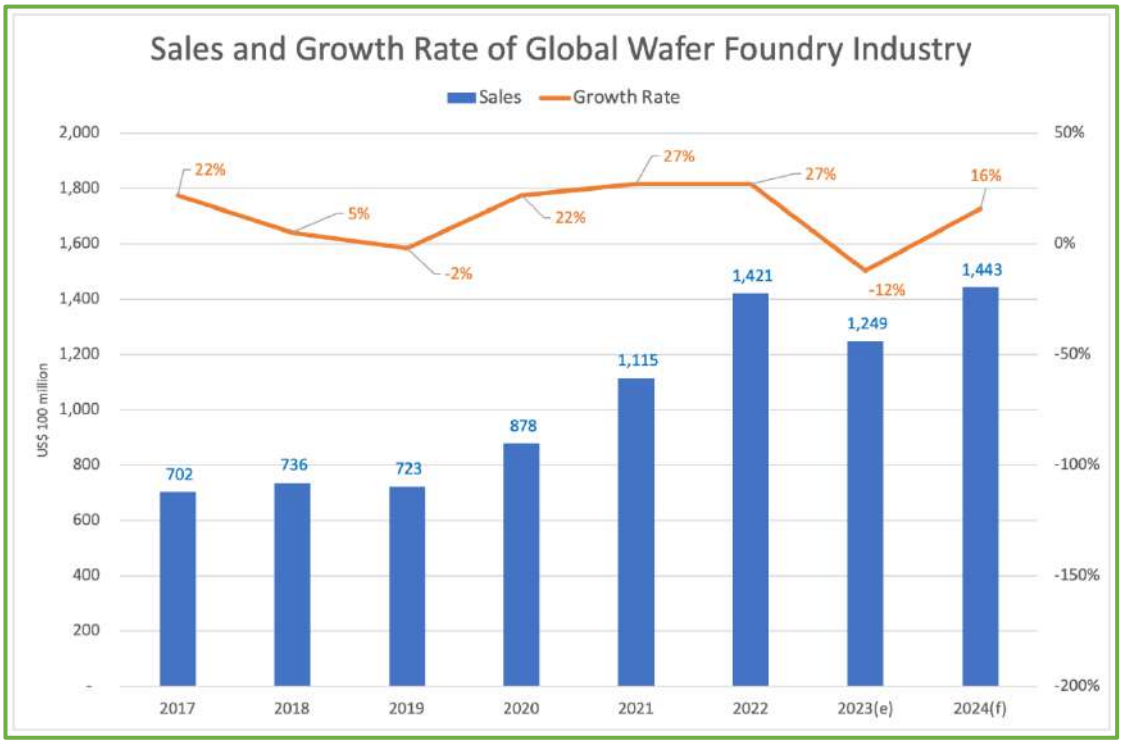
Figure 8 shows the growth prospects of the global semiconductor market for 2011 to 2026. According to the World Semiconductor Trade Statistics (WSTS), the global semiconductor market reached US$ 574.1 billion in 2022, an increase of 3.3% compared with 2021.

Due to rising inflation and weak end market demand in 2023, the latest WSTS report predicts that the global semiconductor market would decline by 9.4% in 2023, with the value of the global semiconductor market falling to US$ 520.1 billion.

In 2024, a robust recovery in semiconductor sales is forecasted, with projections indicating a 13.1% increase, reaching a valuation of US$ 588.4 billion. This growth is expected to be mainly driven by the memory industry. In 2024, the memory industry is predicted to grow at an annual rate of 44.8%,

with output value rising to approximately US$ 130 billion. Other categories including discrete components, test components, analog components, logic components and micro components are also expected to show positive single-digit growth rates.

Figure 9: Sales and Growth Rate of Global Wafer Foundry Industry

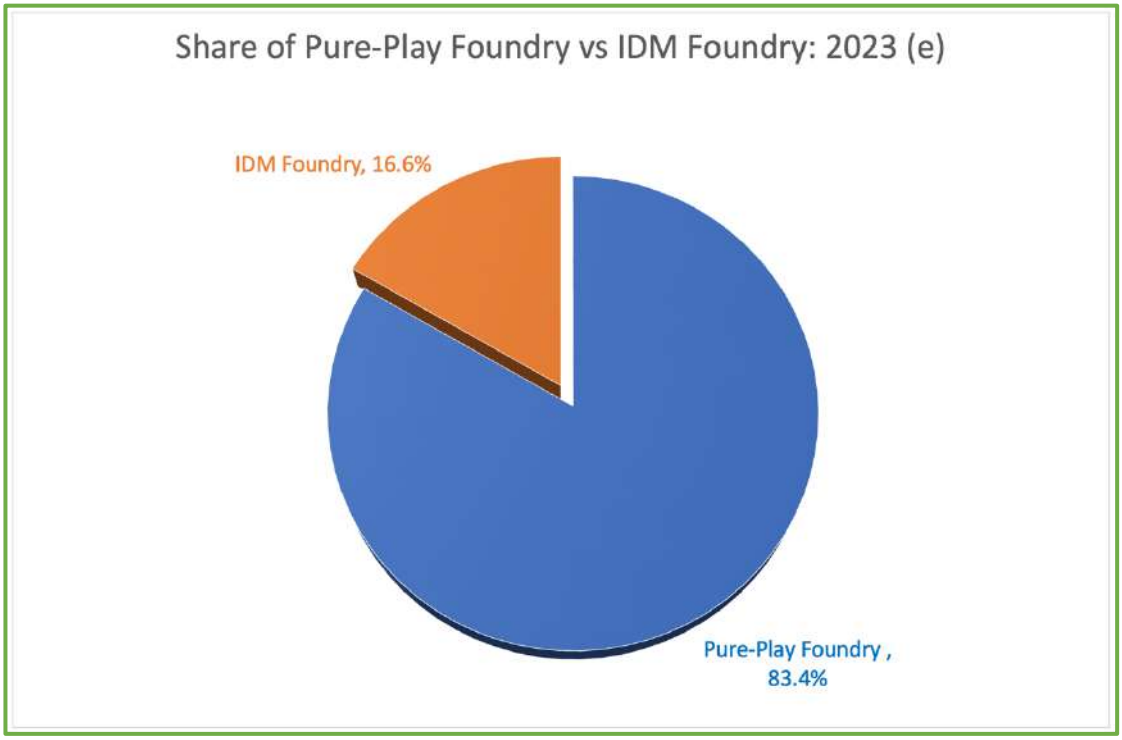


Source: Hui-Hsiu Huang, "Global Semiconductor Foundry Industry Status in 2023," IEK, ITRI, December 19, 2023, p.1.

Figure 9 depicts the sales and growth rate of the global wafer foundry industry from 2017 to 2024 (forecasted). The global wafer foundry revenue reached US$ 142.1 billion in 2022. However, due to macroeconomic uncertainties and rising US-China trade tensions, global foundry revenue is projected to show a decline in 2023. Specifically, the 2023 global foundry revenue is expected to fall 12% to US$ 124.9 billion.

In 2024, with the recovery of semiconductor demand, 5G and high-performance computing (HPC) applications taking off, electronics and automobiles coming with increasing silicon contents, electronics brands and system integrators undertaking in-house chip R&D and IDMs continuing to outsource chip production, the global foundry revenue is expected to grow 16% and hit US$ 144.3 billion.

Figure 10: Share of Pure-Play Foundry vs IDM Foundry: 2023 (e)



Source: Hui-Hsiu Huang, "Global Semiconductor Foundry Industry Status in 2023," IEK, ITRI, December 19, 2023, p.2.

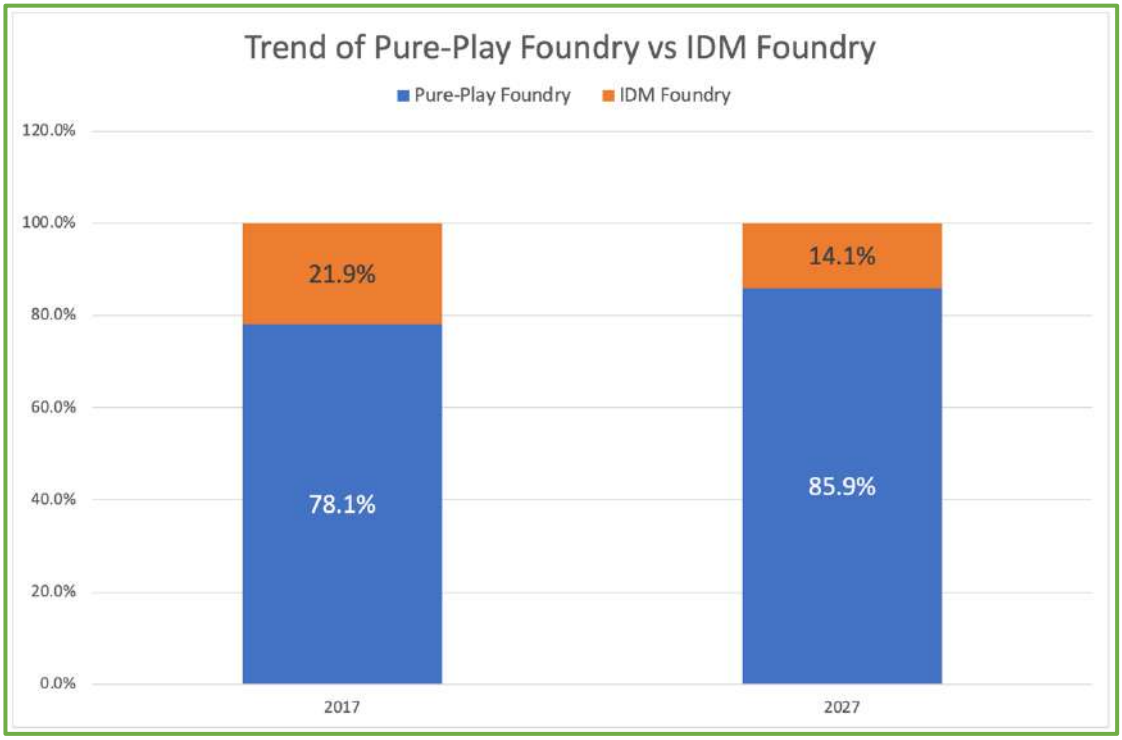
Figure 10 shows the market share of pure-play foundry companies versus IDM foundry companies. In 2023, the pure-play foundry companies are expected to dominate the market with an 83.4% share.

IC Insights defines a pure-play foundry as a company that does not offer a significant number of integrated circuit (IC) products of its own design, but instead focuses on producing ICs for other companies. Examples of pure-play foundry companies include TSMC, GlobalFoundries, United Microelectronics Corporation (UMC), and Semiconductor Manufacturing International Corporation (SMIC).[36]

Integrated device manufacturer (IDM) foundries, on the other hand, are defined as those companies that offer foundry services in addition to manufacturing their own ICs. Examples of IDM foundry companies are Samsung and Intel.[37]

[36] IC Insights, "Pure-Play Foundry Market On Pace For Strongest Growth Since 2014," September 22, 2020.
[37] Ibid.

Figure 11: Trend of Pure-Play Foundry vs IDM Foundry



Source: Hui-Hsiu Huang, "Global Semiconductor Foundry Industry Status in 2023," IEK, ITRI, December 19, 2023, p.2.

Figure 11 shows the trend of pure-play foundry companies versus IDM foundry companies for 2017 to 2027. From 2017 to 2027, the role of IDM foundry companies is expected to shrink while that of the pure-play foundry companies to grow.

In 2027, it is forecasted that IDM foundry companies will see their share shrink 7.8 percentage points, from 21.9% of the foundry market in 2017 to 14.1% in 2027. Meanwhile the pure-play foundry companies are likely to see its share of the market grow by 7.8 percentage points, from 78.1% in 2017 to 85.9% in 2027.

Figure 12: Global Top 10 Wafer Foundry Companies: 2023(e)

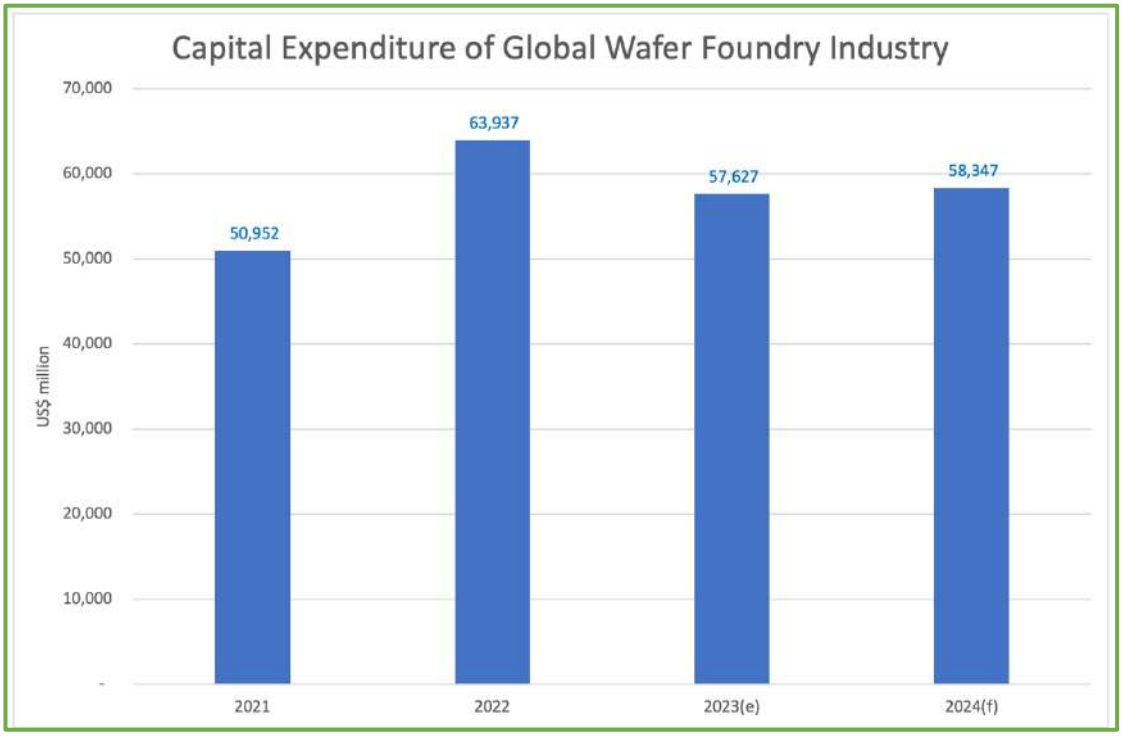
Ranking	Company	Share	Growth Rate
1	TSMC	55%	-10%
2	Samsung	14%	-23%
3	GlobalFoundries	6%	-8%
4	UMC	6%	-20%
5	SMIC	5%	-12%
6	Huahong Group	3%	5%
7	Powerchip	1%	-37%
8	Tower	1%	-14%
9	Vanguard	1%	-20%
10	Nexchip	1%	-10%

Source: Hui-Hsiu Huang, "Global Semiconductor Foundry Industry Status in 2023," IEK, ITRI, December 19, 2023, p.3.

Figure 12 shows the top ten wafer foundry companies in 2023. TSMC leads the list with a 55% share of the global wafer foundry market. Samsung comes a distant second, with a 14% share of the global wafer foundry market. GlobalFoundries and UMC each has a 6% share of the global foundry market, with the former in third place and the latter in fourth position. China's biggest foundry company, SMIC, holds a 5% share of the wafer foundry market and is placed at fifth position.

Overall, other than the Huahong Group, all the foundry companies are expected to see a decline in their growth rate in 2023. The decline is attributed to softening demand for semiconductors as well as challenging global macroeconomic and geopolitical factors.

Figure 13: Capital Expenditure of Global Wafer Foundry Industry



Source: Hui-Hsiu Huang, "Global Semiconductor Foundry Industry Status in 2023," IEK, ITRI, December 19, 2023, p.5.

Figure 13 shows the capital expenditure of the global wafer foundry industry. The capital expenditure of the global wafer foundry industry in 2022 was US$ 63.9 billion. However, due to macroeconomic uncertainties and rising US-China trade tensions, the expenditure is projected to show a decline of 9.8% in 2023. In 2024, the global foundry industry is expected to increase its capital expenditure as economic prospects improve.

Figure 14: Capital Expenditure of Global Top 4 Pure-Play Foundry Companies

Unit: US$ million

	2020	2021		2022		2023(e)	
	Amount	Amount	Growth Rate	Amount	Growth Rate	Amount	Growth Rate
TSMC	17,240	30,043	74%	36,270	21%	32,000	-12%
SMIC	5,733	4,516	-21%	6,350	41%	7,500	18%
UMC	952	1,755	84%	2,710	54%	3,000	11%
GlobalFoundries	449	1,662	270%	3,059	84%	2,000	-35%

Source: Hui-Hsiu Huang, "Global Semiconductor Foundry Industry Status in 2023," IEK, ITRI, December 19, 2023, p.6.

Figure 14 shows the capital expenditure of the world's top four pure-play foundry companies. TSMC is consistently the top spender in capital expenditure, with a CapEx spending of US$ 17.2 billion in 2020, US$ 30.0 billion in 2021, US$ 36.3 billion in 2022, and an estimated reduced spending of US$ 32.0 billion in 2023. Second-placed SMIC has seen its capital expenditure increase, from US$ 5.7 billion in 2020 to US$ 7.5 billion in 2023. Similarly, UMC has seen its capital spending steadily increase over the years, before reaching a high of US$ 3 billion in 2023. Fourth-placed GlobalFoundries saw a fall by 35% of its capital expenditure from US$ 3.1 billion in 2022 to US$ 2.0 billion in 2023.

TAIWAN TRENDS

Figure 15: Output Value of Taiwan's IC Design Industry by Quarter

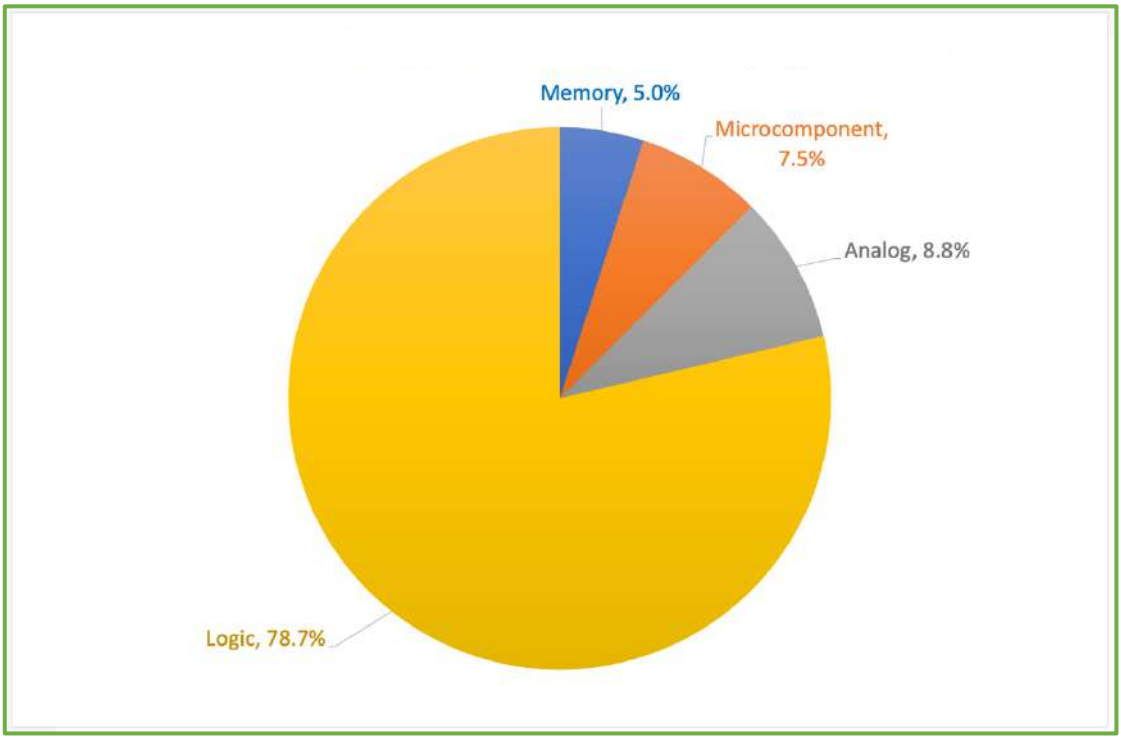
Source: Shu-Ting Chung," 2023 Q3 Industry Dynamics of IC design industry in Taiwan," IEK, ITRI, December 19, 2023, p. 1.

Figure 15 shows the output value of Taiwan's integrated circuit (IC) design industry by quarter, from the third quarter of 2021 to the third quarter of 2023.

With inventories along the supply chain gradually returning to normal levels, and a peak period spike in the end market demand for mobile phones and other communication electronic products and consumer electronics products, Taiwan's IC design industry has seen significant growth for two consecutive quarters in 2023. Additionally, reduced production restoring the equilibrium in the NAND Flash market and stabilizing prices have directly driven the revenue growth of related controller chips.

In the third quarter of 2023, the output value of Taiwan's IC design industry reached NT$ 288 billion (US$ 9.3 billion). This represents an increase of 7.3% from the previous quarter but a decrease of 3.0% from the same period last year.

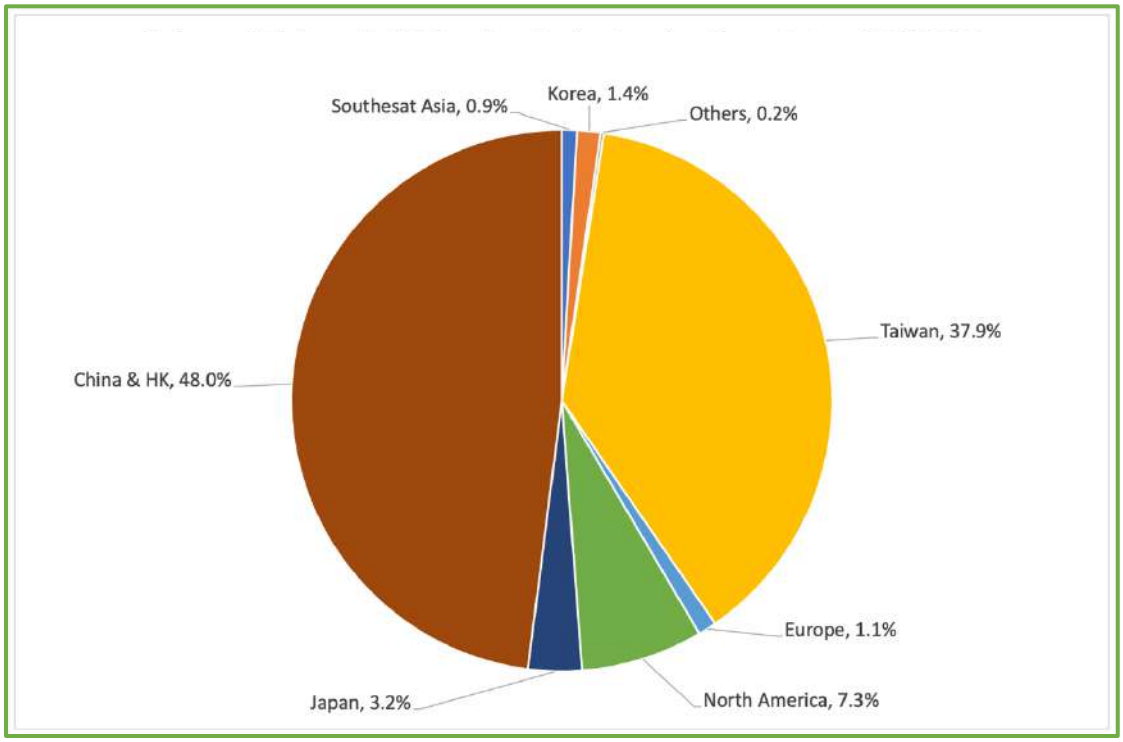
Figure 16: Share of Revenue of Taiwan's IC Design Industry by Products



Source: Shu-Ting Chung," 2023 Q3 Industry Dynamics of IC design industry in Taiwan," IEK, ITRI, December 19, 2023, p. 2.

Figure 16 shows the revenue breakdown of Taiwan's IC design industry by product type in the third quarter of 2023. For Taiwan's IC design industry, logic chips form its largest market and account for 78.7% of its revenue. The main applications of the logic chips include mobile phone chips, network chips and display drivers. Analog chips, which are essential in power management and audio processing, among other uses, account for 8.8% of the industry's revenue. Microcomponents such as Microcontroller Units (MCU), Microprocessor Units (MPU), and Digital Signal Processors (DSP) account for 7.5% of the industry's revenue. Memory chips are its smallest market, contributing to only 5% of the revenue of Taiwan's IC design industry.

Figure 17: Share of Sales of Taiwan's IC Design Industry by Countries: 2023Q3



Source: Shu-Ting Chung," 2023 Q3 Industry Dynamics of IC design industry in Taiwan," IEK, ITRI, December 19, 2023, p. 3.

In the third quarter of 2023, Taiwan's IC design industry is still dominated by customers selling to China/Hong Kong, with the Chinese/Hong Kong market accounting for 48.0% of sales. Taiwan's domestic market accounted for 37.9% of its IC design industry sales. Sales to customers in North America, Japan and Europe accounted for 7.3%, 3.2% and 1.1% respectively.

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SPECIAL FEATURE:

ADVANCED SEMICONDUCTOR ENGINEERING (ASE)

Article contributed by ASE Singapore

About ASE

Advanced Semiconductor Engineering, Inc, (a member of ASE Technology Holdings Co., Ltd. NYSE: ASX, TWSE: 3711) or ASE, as widely known in the semiconductor industry, was founded in Kaohsiung, Taiwan in 1984. The company is a leading semiconductor packaging and testing service provider with manufacturing facilities and field sales operations spanning Asia, North America, and Europe.

Manufacturing Facilities around the World

- *ASE: Kaohsiung, Chungli, Wuxi, Shanghai (Material), ISE labs China, Japan, Korea, Singapore, Malaysia, and ISE Labs*
- *SPIL: Da Fong, Chung Shan, Zhong Ke, Zhong Gong, Hsinchu, Changhua, and Suzhou*
- *USI: Nantou, Zhangjiang, Kunshan, Jinqiao, Huizhou2, Mexico and Asteelflash facilities in China, Czech Rep, France, Germany, Mexico, Poland, Tunisia, UK and USA*

ASE's role in the Semiconductor Value Chain | Leadership through Innovation in Advanced Packaging and Heterogeneous Integration Technologies

Packing more transistors on a monolithic IC is becoming more complex and expensive at each node. The cost of manufacturing chips at the fab level has continued to rise exponentially as process nodes fall. As such, a collaborative effort from all players across the semiconductor eco-system is necessary to address challenges facing these fundamental physical limits. Innovation in semiconductor packaging has always been pivotal to meeting the demands of smaller, faster, higher performance and lower power chip applications.

ASE is a primary architect of Heterogeneous Integration (HI) - the technology that integrates separately manufactured components into a higher-level assembly (System-in-Package or SiP) that in the aggregate provides enhanced functionality and improved operational characteristics. HI is now the key pillar in the advancement of integrated systems for greater intelligence and connectivity, higher bandwidth and performance, and lower latency and power per function, all at a more manageable cost.

In our data centric era, demand for innovative package and IC co-design, cutting-edge wafer level fabrication processes, sophisticated packaging technologies, and comprehensive product and testing solutions has never been greater. The semiconductor market is poised for another decade of growth and projected to surpass US$1 trillion in value by 2030. Behind this exponential growth is data generation from devices used across Artificial Intelligence (AI), Machine Learning (ML), 5G Communications, High Performance Computing (HPC), Internet-of-Things (IoT), and Automotive applications. The role of packaging has become increasingly critical, as applications call for solutions to enable higher performance, greater functionality, and improved power, while meeting stringent cost parameters. The rising adoption of chiplet-based co-designs is further fueling demand for multi-chip integration into a single package.

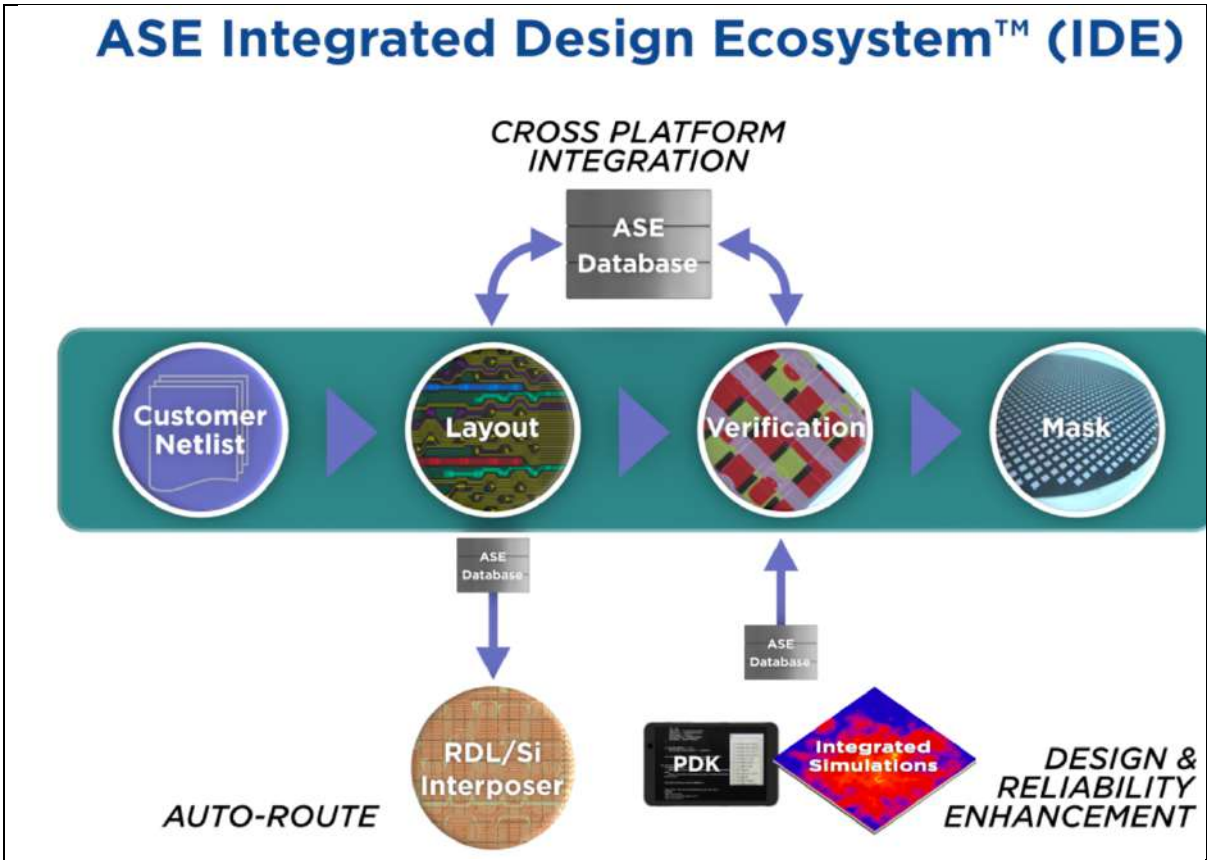
In June 2022, ASE launched the VIPack™, an advanced packaging platform designed to enable vertically integrated package solutions. VIPack™ represents ASE's next generation of 3D heterogeneous integration architecture that extends design rules and achieves ultra-high density and performance. The platform leverages advanced redistribution layer (RDL) processes, embedded integration, and 2.5D and 3D technologies to help customers achieve unprecedented innovation when integrating multiple chips within a single package.

The VIPack™ platform comprises six core packaging technology pillars supported by a comprehensive and integrated design ecosystem. These technology pillars include ASE's high density RDL based FOPoP, FOCoS, FOCoS-Bridge, and FOSiP as well as TSV based 2.5D/3D IC and Co-Packaged Optics processing capabilities.

VIPack™ by ASE: an advanced packaging platform designed to enable vertically integrated package solutions.

Today's frontline chiplet and heterogeneous integration developments are pushing technology boundaries and elevating demand for innovative design flows and circuit-level simulations to accelerate complex design architectures. To that end, on October 2023, ASE introduced the Integrated Design Ecosystem™ (IDE), a collaborative design toolset that is optimized to systematically boost the advanced package architecture across our VIPack™ platform. This novel approach allows a seamless transition from single die SoC to multi-die disaggregated IP blocks including chiplets and memory for integration using 2.5D or advanced fanout structures.

The IDE enables design efficiencies up to 50% and sets new standards for quality and user experience. Integrating innovative package design tool capabilities into ASE's workflow has resulted in significant cycle time reduction while lowering customer costs. Enhanced features of IDE include cross platform interaction encompassing layout and verification, advanced RDL and silicon interposer auto routing with embedded design rule checking (DRC), and Package Design Kit (PDK) implementation in the design workflow.



ASE's Integrated Design Ecosystem™ (IDE) is a collaborative design toolset to boost the VIPack™ advanced package architecture

Contributing to the continuous progress and innovation of the industry as a whole, is the responsibility of all players across the industry chain. ASE is actively involved in many semiconductor and cross-industry organizations that advance policies and agendas to help the industry and community advance, grow and address common challenges. In line with the company's developments in advanced packaging and 3D integration for chiplets, ASE is heavily involved in defining chiplet technology standards through the UCIe (Universal Chiplet Interconnect express https://www.uciexpress.org/) platform.

Industry 4.0 | Sustainable Manufacturing through Smart and Digital Transformation

Market shifts in customer requirements as well as the advent of 5G wireless technologies have given rise to smart manufacturing and the acceleration of Industry 4.0 at ASE. Smart Factories represent the future of our industry and are an integral part of ASE's business operations. ASE's strategy is to leverage on AI, Big Data and Smart Automation to achieve full

digital transformation and harness the power of smart manufacturing to increase productivity, add more value to the supply chain and strive for near perfection.

In December 2022, ASE's wafer bumping facility in Kaohsiung was formally inducted into the World Economic Forum Global Lighthouse Network (GLN), a community of manufacturing sites and value chains that are leaders in the adoption of Fourth Industrial Revolution (4IR) cutting edge technologies. In the bumping operation, there are more than 100 process steps compared with traditional IC packaging operations. ASE Kaohsiung successfully deployed 4IR technologies across hundreds of complex fabrication processes, improving manufacturing yields and accuracy that resulted in a 67% increase in output and a 39% reduction in order lead time. As one of the 132 GLN factories in the world, ASE has truly demonstrated the company's incredible foresight, and strategic thinking in the integration of 4IR technologies into its smart manufacturing blueprints.

Digital technology is transforming workplaces at ASE. The company is not only applying digital technologies to enhance the efficiency and productivity of its operations, but also using it to improve workplace safety. For instance, AIoT and edge computing technologies are used to perform IoT data collection and AI predictive analytics on production equipment to pre-determine anomalies. This approach allows ASE to plan ahead for maintenance and repairs and minimizes disruptions from shutdowns. It also ensures operation stability and increases energy efficiency as energy wastage associated with obsolete or malfunctioning equipment is vastly reduced. Through the use of XR (Extended Reality) technology which combines both VR (Virtual Reality) and AR (Augmented Reality), ASE is able to simulate equipment performance under certain conditions without disrupting the actual production lines. This has allowed its employees to undergo professional skills training in a safe and secure environment, further improving the efficiency and workplace safety and health. By the beginning of 2024, ASE has already established more than 40 smart factories globally, with the majority in Taiwan.

Race to Net Zero through Climate Science

Extreme climate impacts the world around us, with global warming causing greater disruptions to the environment and livelihoods. Greenhouse gas emissions from human activity is a primary driver of climate change and the semiconductor industry has taken major steps to address and reduce its carbon footprints. ASE has set absolute GHG reduction targets for 2030 and is on track to achieve its ambition of Net Zero by 2050 through an extensive carbon reduction framework that includes:

- Establishing GHG reduction targets and validation by the Science Based Targets initiative (SBTi), an organization promoting best practices in emissions reductions and net-zero targets in line with climate science.
- Transitioning to renewable energy usage including the establishment of solar power generation capabilities and procuring renewable energy and certificates.
- Collaborative efforts with supply partners to improve energy efficiencies and reduce emissions across the value chain.
- Recycling, reducing, and reusing material to prolong life cycles and reduce waste generation that contributes to environmental damage.
- Membership, sponsorship and directing resources to support meaningful external programs. Eg. ASE is a founding member of the SEMI Semiconductor Climate Consortium (SCC) and Energy Collaborative.

Challenges, Opportunities, and a Future-proof Business Model

While a certain level of normalcy has returned since the easing of the pandemic, our world is still beset with multiple challenges. From the Russo-Ukrainian war, Israeli-Palestinian conflict to geopolitical tensions, inflation, and the climate crisis, prospects for global growth remain uncertain. Nevertheless, semiconductors continue to play a crucial role in the global economy. Most importantly, the rise of new technologies especially the advent of artificial intelligence, vehicle electrification, high performance computing and more, will continue to drive, if not accelerate, semiconductor growth. As a key player in the semiconductor manufacturing sector, ASE is

committed to applying a corporate strategy that balances the company's innovation and digital transformation based on a sustainable and human-centric approach.

In the IC packaging and test business, technology and service quality are a given. What makes an organization stand out is its value and contribution to sustainable development. ASE's ESG performance has been widely recognized by major international rating agencies over the past decade. Amongst which, was the recognition for the 8th year in a row on the Dow Jones Sustainability Indices (DJSI), topping the list with the highest scores on the Semiconductors and Semi Equipment Industry Group. The recognition on the DJSI serves as an impetus for the company to set even higher standards for ESG, embedded into a robust business model going forward.

ASE's Global Footprint | ASE Malaysia and ASE Singapore

To build greater resilience, and strengthen its core competitiveness, ASE's business model is guided by a strategic focus on long term goals and achievements in technology innovation, and smart and sustainable developments. ASE's global footprint is well-positioned to respond to increasing demands to serve different geographical markets and customer needs, as well as risk diversification. Besides strengthening its advanced packaging and testing capabilities in Taiwan, the company aims to continue expanding its manufacturing capacities in China, Japan, Korea, Malaysia, Singapore, and other countries.

In November 2022, ASE announced the expansion plans of the assembly and testing facility in Penang, Malaysia (ASEM), investing US$ 300 million over a period of 5 years to expand production floor space, procure advanced equipment, and train and develop more engineering talent. Construction has already begun, and the new facility will comprise 2 buildings (Plants 4 and 5) with a built-up area of 982,000 square feet. Upon completion, ASEM will have a total of 2 million square feet of floor space, representing a two-fold increase from the current floor space. The new facility will continue to focus on high volume packaging product types

including copper clip and image sensors, with plans for more advanced packaging technologies in the pipeline.

ASE Malaysia's expansion plans will comprise 2 new buildings scheduled to be completed by 2025

ASE Singapore is a premier IC chip testing service provider, established since 1998. Today, the facility serves global semiconductor customers who supply cutting edge chips for the mobile, computing, networking, and automotive market segments. The Singapore facility spans over 320,000 square feet of manufacturing and office space, providing high quality semiconductor chip testing, wafer probing and backend wafer level assembly services. For 4 years in a row since 2020, ASE Singapore has earned the title of 'Singapore Best Employers', a large-scale annual survey conducted by the Straits Times and Statista, that assesses the attractiveness of organizations in Singapore based on an independent employee survey.

ASE Singapore celebrating recipients of the long service awards in 2024.

For more information about ASE Inc, please visit ase.aseglobal.com, and subscribe to LinkedIn/ X @aseglobal.

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